Printed Page:-04 **Subject Code:- BEC0403**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech (ECE-Working Professional)

SEM: II - THEORY EXAMINATION (2024 - 2025)

Subject: CMOS Digital Integrated Circuit

Time: 3 Hours **Max. Marks: 100**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* ***three Sections -A, B, & C.*** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION-A 20

1. Attempt all parts:-

1-a. What is voltage condition in Linear region of n-type of MOSFET? (CO1, K1) 1

(a) VGS>VTH

(b) VGS<VTH

(c) VGS=VTH

(d) VGS =0

1-b. What is the name of MOSFET with n-channel? (CO1, K2) 1

(a) PMOS

(b) NMOS

(c) CMOS

(d) BiCMOS

1-c. Which device has one input and many outputs? (CO2,K2) 1

(a) Multiplexer

(b) Demultiplexer

(c) Counter

(d) Flip flop

1-d. In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance? (CO2, K2) 1

(a) Static dissipation

(b) Dynamic dissipation

(c) Both a and b

(d) None of the above

1-e. The truth table for an S-R flip-flop has how many valid entries? (CO3,K2) 1

(a) 1

(b) 2

(c) 3

(d) 4

1-f. A full adder can be made out of _____. (CO3,K6) 1

(a) Two half adders

(b) Two half adders and a OR gate

(c) Two half adders and a NOT gate

(d) Three half adders

1-g. The output of domino CMOS gate is low at the beginning of _____. (CO4, K4) 1

(a) Precharge Phase

(b) Evaluation Phase

(c) Dynamic Phase

(d) Static Phase

1-h. In pseudo-NMOS circuit, PMOS transistor is not driven by any signals, it is always _____. (CO4, K2) 1

(a) On

(b) Off

(c) In cut-off region

(d) In breakdown region

1-i. Delay between the shortest path and the longest path in the clock is called _____. (CO5,K2) 1

(a) Global skew.

(b) Useful skew.

(c) Local skew.

(d) Slack.

1-j. Which among the following operation/s is/are executed in physical design or layout synthesis stage? (CO5,K1) 1

(a) Placement of logic functions in optimized circuit in target chip

(b) Interconnection of components in the chip

(c) Both a and b

(d) None of the above

2. Attempt all parts:-

2.a. Explain threshold voltage of a MOSFET. (CO1,K2) 2

2.b.	Differentiate the enhancement-type and depletion-type MOSFET. (CO2,K2)	2
2.c.	Explain working of CMOS Half adder with the help of a neat diagram. (CO3,K3)	2
2.d.	Write two major disadvantges of Pseudo-NMOS logic. (CO4,K2)	2
2.e.	What do you understand by Floorplanning? (CO5,K2)	2

SECTION-B 30

3. Answer any five of the following:-

3.a.	Derive the expression for maximum depletion region depth when MOS capacitor is in inversion region and also mention the polarity of externally applied voltage to it. (CO1,K5)	6
3.b.	What do you mean by MOSFT capacitance and explain different types of MOS capacitances? (CO1,K2)	6
3.c.	Derive the expression for dynamic power dissipation in CMOS inverter. (CO2,K4)	6
3.d.	What do you mean by noise margin? How a greater noise margin helps in reducing the external noise effects in digital circuits? (CO2,K2)	6
3.e.	Draw the CMOS implementation of Y = [(A.D+B)C+E]' (CO3,K6)	6
3.f.	What is pass transistor? Explain how it passes Logic '0' and Logic '1'. (CO4, K2)	6
3.g.	Explain in brief the Power routing. (CO5,K2)	6

SECTION-C 50

4. Answer any one of the following:-

4-a.	Explain in detail with neat diagram (i) Drain induced barrier lowering (DIBL) (ii) Career velocity saturation.(CO1,K2)	10
4-b.	Derive the expression for drain current in linear region of MOSFET. (CO1,K5)	10

5. Answer any one of the following:-

5-a.	Draw and explain the voltage transfer characteristics (VTC) of CMOS inverter. (CO2, K2)	10
5-b.	Discuss the transient analysis of CMOS inverter and explain the followings parameters in brief. (i) Propagation delay (ii) fall time (iii) rise time. (CO2, K2)	10

6. Answer any one of the following:-

6-a.	Explain Clocked CMOS SR Latch based on NAND gate in detail.Verify It's truth table. (CO3, K2)	10
6-b.	Implement CMOS full adder and explain its working. Write output equations for sum and carry outputs. (CO3, K5)	10

7. Answer any one of the following:-

7-a.	Implement the 2-input NOR gate using static CMOS and dynamic CMOS logic. (CO4,K6)	10
7-b.	Explain Cascading problem in dynamic CMOS logic and how it is removed? (CO4,K2)	10

8. Answer any one of the following:-

8-a.	Compare SRAM and DRAM in terms of cell design, speed, power, density, and applications. (CO5,K2)	10
8-b.	What is Placement?Write any of the placement algorithm and explain it's goals and objectives. (CO5,K2)	10

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